Spectra IP CORE ORB High Performance Message Processing for FPGAs

Spectra IP Core ORB (ICO) is a hardware implementation of CORBA's GIOP protocol and is part of ADLINK's Spectra Common Data Bus (CDB) range of high performance embedded messaging solutions. ICO provides an implementation of the GIOP protocol at the gate level and by supporting a highly optimized subset of ORB features it is now possible to provide a single, seamless industry standard data protocol across processor architectures. Specifically designed to support high performance Software Defined Radio (SDR) applications based on the Software Communications Architecture (SCA), ICO can just as easily be used as a general purpose integration solution for use in embedded FPGA applications with no SCA requirements.

FPGA Integration Has Never Been Easier

ICO is used as a GIOP message-processing engine for FPGAs and ASICS, enabling a standard protocol to be run across multiple processor architectures (GPP, DSP and FPGA). This reduces the need to support custom protocols and proprietary interfaces. These non-standard types of interface in an FPGA environment are often referred to as Hardware Abstraction Layers (HALs). The major problem with the HAL approach is that they are difficult to implement and maintain and require the hardware developer to understand the low-level details of each proprietary messaging protocol. They also need to be re-written if the underlying hardware changes reducing application portability and increasing time to market and cost for new applications.

ICO further eliminates the need to embed general purpose processing cores into FPGAs in order to offer software ORB capability. Although a viable approach, this approach tends to require significant gate count and memory utilization and generally these processing cores cannot be clocked fast enough to deal with the ever-increasing performance requirements of SDR applications. ICO has been written in portable VHDL that can be synthesized onto any FPGA or ASIC device.

The ICO development environment consists of:

- The ICO IP core message processing engine
- IDL to VHDL Compiler
- A number of board specific example transports
- Supporting user documentation

ICO was designed to be modular and configurable. Figure 1 below provides an illustration of ICO's architecture. Figure 1 below provides an illustration of ICO's architecture. Components shown in yellow are provided as part of the ICO core, components in blue are generated by the IDL to VHDL compiler for each specific design.

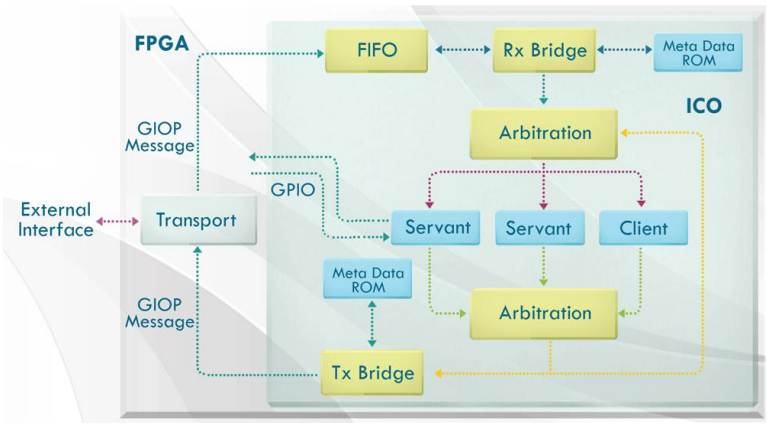

Figure 1 – ICO Architecture

Super Fast Message Processing

ICO processes CORBA GIOP messages at hardware speeds which is hundreds of times faster than can be achieved with a conventional software ORB. For example, for a simple interface that supports a two-way synchronous CORBA call and is passed a payload of 1024 bytes as an IN parameter (implemented on a Altera Cyclone III FPGA, clocked at 160MHz), it takes approximately 1.88μS to process the message from the first byte of the incoming message being read by ICO from the transport to the last byte of the reply message being written to the transport by ICO. This represents a data throughput of over 540Mbytes/sec. At higher clock speed and with a more powerful FPGA, for example an Altera Stratix IV, a data throughput rate of over 1Gbyte/sec can be achieved.

Key Features

- Supports GIOP version 1.0 protocol
- Processes CORBA requests
  - One way operations
  - Two way operations
- Support for CORBA clients and servers
  - Servants implemented on FPGA in VHDL
  - Clients can be internal to the FPGA written in VHDL or external to FPGA (e.g., on a GPP or DSP) implemented by a conventional software application
  - No arbitrary restriction on the number of clients and servants that can be supported on the FPGA
- IDL compiler support
  - Supports IDL to VHDL language mapping and will auto generate VHDL equivalent of CORBA stubs and skeletons allowing ICO to be easily connected to servants implementing waveform logic
  - Based on CORBA 3 grammar, but only supporting a subset of data types and constructs
    - Simple data types - Char, Octet, Boolean, Short, Unsigned Short, Long, Unsigned Long, Long Long, Unsigned Long Long, String
    - Any type (of simple data types)
    - Object type
    - Enumerated types
    - Constructed data types
      - Struct
      - Sequence
      - Array
  - CORBA exceptions support
    - User exceptions
    - System exceptions
- Pluggable and open transport interface allows user-defined custom transports to be plugged into ICO
- Written in pure VHDL and portable across FPGA devices

FPGA Device Coverage

Spectra ICO was written in 100% VHDL and was designed to be portable so that a wide range of FPGAs and ASICS can be supported. ICO currently supports the leading FPGA devices from Xilinx and Altera. For the most up to date list of supported FPGAs, please contact ADLINK.

SCA Everywhere

Spectra CDB provides the only SCA-compliant CORBA solution that is available across not only GPP, but also DSP and FPGA processing environments. This complete processor coverage has been made possible through the development of specialized CORBA middleware technology designed to support DSPs and FPGAs with Spectra ICO. ADLINK has pioneered the use of lightweight ORB technology for DSPs and advanced hardware ORB technology for FPGAs. The Spectra approach helps decouple SDR applications from the underlying hardware, making hardware upgrades much more straightforward as well as maximizing waveform application portability.

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Leading EDGE COMPUTING

Complementary SDR Products

Spectra ICO is part of the most complete family of SDR products and technologies designed to support all of your SCA SDR development needs.

Summary of Spectra ICO Benefits

- High performance standards based messaging for FPGAs
- Greatly simplifies FPGA application integration
- Helps support FPGA application portability
- High throughput low latency messaging solution
- Helps reduce time to market for new FPGA applications
- Low footprint—efficient use of available FPGA resources
- Available as part of a complete range of complementary SDR products
- Can support a unified messaging protocol across GPP, DSP and FPGA processing elements
- Can support a broad range of FPGA devices from the leading vendors
- No export restrictions - not subject to International Traffic in Arms Regulations (ITAR) or Joint Tactical Radio System (JTRS) export restrictions

For More Information

For further information regarding Spectra ICO or any SDR products, please e-mail: ist_info@adlinktech.com or visit: ist.adlinktech.com